CLAIMS:

1. An amplifier circuit comprising:

- a pre-amplifying stage,
- an amplifying stage, and
- identification means for identifying the configuration of the amplifying stage,

which circuit is characterized in that it additionally comprises adaptation means to configure the pre-amplifying stage in such a manner that it supplies the amplifying stage with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.

2. An amplifier circuit as claimed in claim 1, characterized in that the pre-amplifying stage comprises two pre-amplifiers, which are both arranged between two inputs of the amplifier circuit and two inputs of the amplifying stage, the adaptation means alternately activating one of the two pre-amplifiers and deactivating the other.

3. An amplifier circuit as claimed in claim 2, characterized in that the pre-amplifying stage includes a first pre-amplifier comprising two transistors forming a long-tail pair, having control terminals which are connected to inputs of the amplifier circuit.

4. An amplifier circuit as claimed in claim 2, characterized in that the pre-amplifying stage includes a second pre-amplifier comprising four transistors which, arranged two-by-two, form a first and a second long-tail pair, having control terminals which are connected in parallel to inputs of the amplifier circuit, each long-tail pair having an output connected to one of the inputs of the amplifying stage.

5. An amplifier circuit as claimed in claim 1, characterized in that the identification means of the amplifying stage configuration comprise detection means connected to the outputs of said amplifying stage, said detection means having at least one

output intended to supply a current whose direction is determined univocally by the direction of an output current generated by the amplifier circuit.

6. An amplifier circuit as claimed in claim 5, characterized in that the identification means of the amplifying stage configuration comprise selection means connected to the detection means and having two outputs intended to be energized alternately according to the direction of the current supplied by the outputs of the detection means.

7. An amplifier circuit as claimed in claim 1, characterized in that the adaptation means comprise a flip-flop intended to store information provided by the identification means, a logic output of said flip-flop being coupled to the pre-amplifying stage.

8. A tuner characterized in that it includes an amplifier circuit as claimed in claim 1.

9. A receiver for receiving radioelectric signals, characterized in that it includes a tuner as claimed in claim 8.

10. A method of optimizing the operation of an amplifier circuit comprising

- a pre-amplifying stage, and
- an amplifying stage,

which method comprises an identification step for identifying the amplifying stage configuration, characterized in that the method additionally includes a configuration step to configure the pre-amplifying stage in such a manner that it supplies the amplifying stage with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.